METHOD FOR SUPPRESSING SHORT CHANNEL EFFECT OF A SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

This application claims the priority benefit of Taiwan application serial no. 91102058, filed February 6, 2002.

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a method for suppressing the short channel effect of a semiconductor device. More particularly, the present invention relates to a method for suppressing the short channel effect by using pocket implantation.

Background of the Invention

[0002] Flash memory is an electrically erasable programmable read-only memory (EEPROM) that is widely used in computer and microprocessor systems for permanently storing information that are repeatedly read, written or erased. Moreover, flash memory can retain information even when power is interrupted. Flash memory is a type of non-volatile memory (NVM), which is small in size, faster in reading/programming speed and consumes less power and energy. Since the erasure of information for a flash memory is accomplished "block-by-block", the operational speed is also faster.

[0003] Figures 1A to 1E are schematic diagrams in a cross-sectional view illustrating the fabrication of a semiconductor device according to the prior art.

[0004] As shown in Figure 1A, a substrate 100 is provided. A gate structure 106 is formed on the substrate 100. The gate structure 106 includes a gate oxide layer 102 and a gate conductive layer 104. Using the gate structure 106 as an implantation mask, an ion implantation 107 is conducted to form a source/drain extension region 108 in the substrate 100 beside the gate structure 106.

[0005] Referring to Figure 1B, a spacer 110 is formed on the sidewall of the gate structure 106. Using the spacer 110 and the gate structure 106 as an implantation mask, an ion implantation 111 is conducted to form a source/drain region 112 in the substrate 100 beside the spacer 110.

[0006] Continuing to Figure 1C, a first thermal process is conducted, wherein the first thermal process is to anneal the source/drain extension region 108 and the source/drain regions 112 in order to repair the lattice defects created during the ion implantation process 107 and 111.

[0007] Referring to Figure 1D, a pocket implantation 114 also known as a halo implantation is conducted to form a pocket doped region 116 under the source/drain extension region 108. The type of dopants implanted in the pocket doped region 116 is different from the type of dopants implanted in the source/drain extension region 108 and in the source/drain region 112. The shallow junction formation is to suppress the short channel effect of the semiconductor device. For a typical N channel metal oxide semiconductor device (NMOS), boron ions are conventionally used to form the pocket doped region 116.

[0008] Continuing to Figure 1E, a second thermal process is conducted, wherein the second thermal process is to anneal the pocket doped region 116 in order to repair the lattice defects created during the pocket implantation 114.

[0009] Although conventionally, methods have been developed to suppress the short channel effect in a semiconductor device. An example of such includes, as discussed above, forming a pocket doped region 116 under the source/drain extension region to suppress the short channel effect. The conventional method, however, fails to consider the fast diffusion of dopants in the pocket doped region to effectively suppress the short channel effect.

[0010] Moreover, in the aforementioned method to suppress the short channel effect in a semiconductor device, a first thermal process is conducted to form the source/drain extension region and the source/drain region. Since the first thermal process repairs the lattice defects formed during the implantation processes 107, 111, the second thermal process, conducted subsequent to the formation of the pocket implantation, will cause the dopants in the pocket doped region to diffuse.

SUMMARY OF THE INVENTION

[0011] The present invention provides a method to suppress the short channel effect of a semiconductor device, wherein the diffusion of dopants in the pocket doped region is mitigated in order to suppress the short channel effect in a semiconductor device.

[0012] The present invention also provides a method to suppress the short channel effect of a semiconductor device, wherein a diffusion of the dopants in the pocket doped region due to the subsequent thermal process is prevented.

[0013] The present invention provides a method to suppress the short channel effect of a semiconductor device. A substrate is provided and a gate structure is formed on the substrate. A first ion implantation process is conducted to form a source/drain extension region using the gate structure as an implantation mask. The dopants used for the first ion implantation process include antimony or arsenic. After this, a spacer is formed on the sidewall of the gate structure, and a second ion implantation process is conducted to form a source/drain region beside the spacer in the substrate. A pocket implantation is conducted to form a pocked doped region under the source/drain extension region, wherein the dopants used for the pocket implantation includes indium. Subsequent to the formation of the pocket doped region, a thermal process is conducted to anneal the source/drain extension region, the source/drain region and the pocket doped region.

[0014] The present invention provides a method to suppress the short channel effect of a semiconductor device, wherein a thermal process is not performed after the formation of the source/drain extension region and the source/drain region. The lattice defects formed during the implantation process are not repaired. The dopants in the pocket doped region are then trapped in the lattice defects to reduce the diffusion of the dopants in the pocket doped region during the subsequent thermal process.

[0015] The present invention provides a method to suppress the short channel effect, wherein indium ions are used to replace the conventional boron ions in forming the pocket doped region. Since indium ions are heavier than boron ions, indium ions diffuse at a slower rate. The diffusion of dopants from the pocket doped region thus reduces.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0018] Figures 1A to 1E are schematic diagrams in a cross-sectional view illustrating the fabrication of a semiconductor device according to the prior art;and

[0019] Figures 2A to 2C are schematic diagrams in a cross-sectional view illustrating the fabrication of a semiconductor device according one embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0020] Figures 2A to 2C are schematic diagrams in cross-sectional view illustrating the fabrication of a semiconductor device according one embodiment of the present invention.

[0021] As shown in Figure 2A, a substrate 200 is provided, wherein the substrate 200 is, for example, a p-type silicon substrate. A gate structure 206 is formed on the

substrate 200. The gate structure 206 includes a gate oxide layer 202 and a gate conductive layer 204, wherein the gate conductive layer 204 is, for example, polysilicon.

[0022] Thereafter, using the gate structure 206 as an implantation mask, an ion implantation process 207 is conducted to form a source/drain extension region 208 in the substrate 200 beside the gate structure 206, wherein the source/drain extension region 208 is implanted with N-type dopants. The N-type dopants include antimony ions or arsenic ions. The implantation energy for the ion implantation process 207 is about 10keV and the dosage of the ion implantation process 207 is about $3x10^{14}/cm^2$.

[0023] As shown in Figure 2B, a spacer 210 is formed on the sidewall of the gate structure 206. The spacer 210 is formed by forming a conformal dielectric layer on the substrate 200, followed by back-etching the conformal dielectric layer.

[0024] After this, using the gate structure 206 and the spacer 210 as an implantation mask, an ion implantation process 211 is conducted to form a source/drain region 212 in the substrate 200 beside the spacer 210. The dopants implanted in the source/drain region are same as those implanted in the source/drain extension region 208. As discussed in the above, the dopants implanted for the source/drain region 212 include antimony ions or arsenic ions.

[0025] Referring to Figure 2C, subsequent to the formation of the source/drain extension region 208 and the source/drain region 212, a pocket doped implantation 214 is conducted to form a pocked doped region 216 under the source/drain extension region 208. The dopants implanted for the pocket doped region 216 includes a p-type dopant. According to the preferred embodiment of the present invention, the dopants used for the pocket doped region 216 includes indium ions. The implantation energy for the pocket

doped implantation process 214 is about 10keV. The dosage of the pocket doped implantation process 214 is about $3x10^{14}/cm^2$. The pocket doped implantation process 214 tilt angle is about 30 degrees.

[0026] After the formation of the pocket doped region 216, a thermal process is conducted to anneal the source/drain extension region 208, the source/drain region 212 and the pocket doped region 216 concurrently to repair the lattice defects formed during the above implantation processes 207, 211, 214. The thermal process is, for example, a rapid thermal process, conducted at a temperature of about 900 degrees Celsius for about 10 seconds.

[0027] Since in the present invention, a thermal process is not performed after the formation of the source/drain extension region 208 and the source/drain region 212, the lattice defects formed during the implantation processes 207, 211 in forming the source/drain extension region 208 and the source/drain region 212 are not repaired. During the subsequent formation of the pocket doped region 216, the implanted indium ions are trapped in the above lattice defects. The diffusion of the indium ions during the subsequent thermal process is effectively suppressed.

[0028] Moreover, since the p-type dopants implanted for the pocket doped region 216 is indium ions and indium ions are heavier than the conventional boron ions. The indium ions thus diffuse at a much slower rate than the boron ions. The indium ions thereby replace the role of the boron ions as the dopants for the pocket doped region to mitigate the diffusion problem in the doped pocket region 216.

[0029] According to the method in suppressing the short channel of the present invention, a thermal process is not conducted after the formation of the source/drain

extension region and the source/drain region. Lattice defects formed during the ion implantation processes are not repaired. The dopants of the subsequently formed pocket doped region are trapped in the lattice defects to reduce the diffusion of dopants in the pocket doped region during the subsequently performed thermal process.

[0030] Additionally, according to the method of the present invention in suppressing the short channel effect, indium ions are used to replace boron ions as the dopants being implanted for the pocket doped region. Since indium ions are heavier than boron ions, the diffusion of dopants in the pocket doped region is retarded.

[0031] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.